

The diagram shows a control system with five numbered inputs/outputs:

- 1**: A horizontal input line from the left entering a circular summing junction.
- 2**: An input line from the top-left entering the summing junction.
- 3**: A rectangular block representing a controller or actuator, receiving the output of the summing junction.
- 4**: A feedback line from the output of the system (after a junction) entering the bottom of the summing junction.
- 5**: The final output line of the system, branching off from the feedback line.

Signs (+) are present at the summing junction and the feedback input to indicate positive feedback.

The diagram illustrates a transmission system (10) consisting of three main processing blocks connected in series. An input signal, indicated by arrow 6, enters the 'OUTER ENCODER' block (labeled 7). The output of the outer encoder is passed to the 'INTERLEAVER' block (labeled 8). The output of the interleaver is then passed to the 'INNER ENCODER' block (labeled 9). Finally, the output of the inner encoder is shown as an output signal, indicated by arrow 10.

FIGURE 1C

FIGURÉ 1C

BER

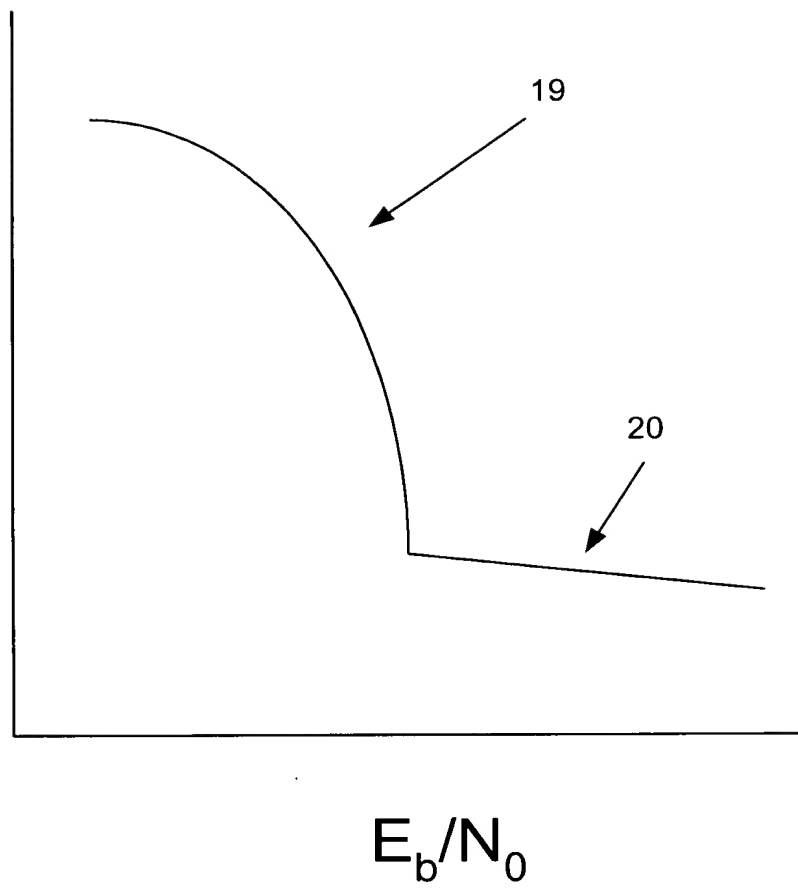
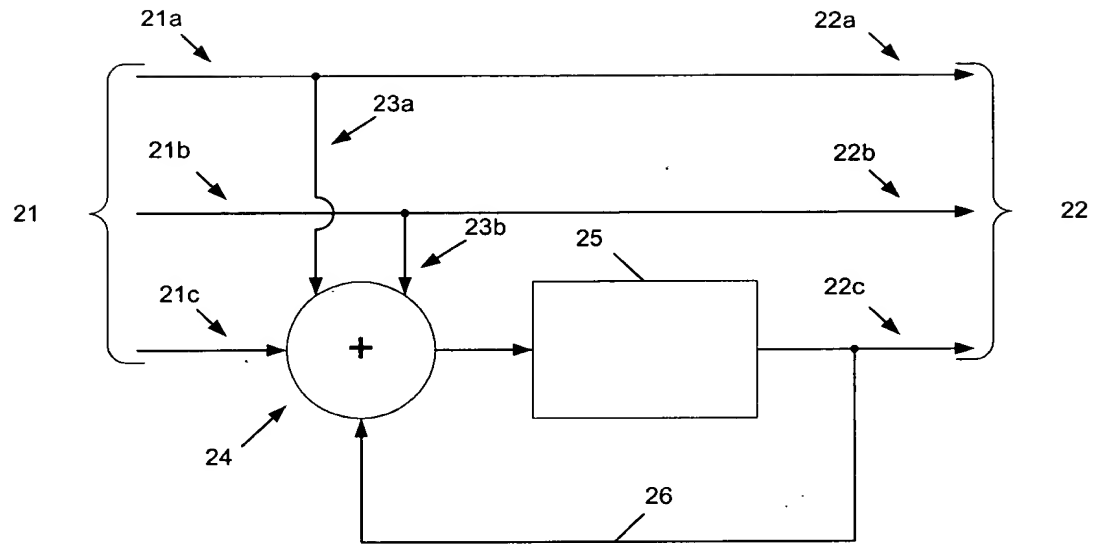


FIGURE 2

FIGURE 3A



• 3



SECRET

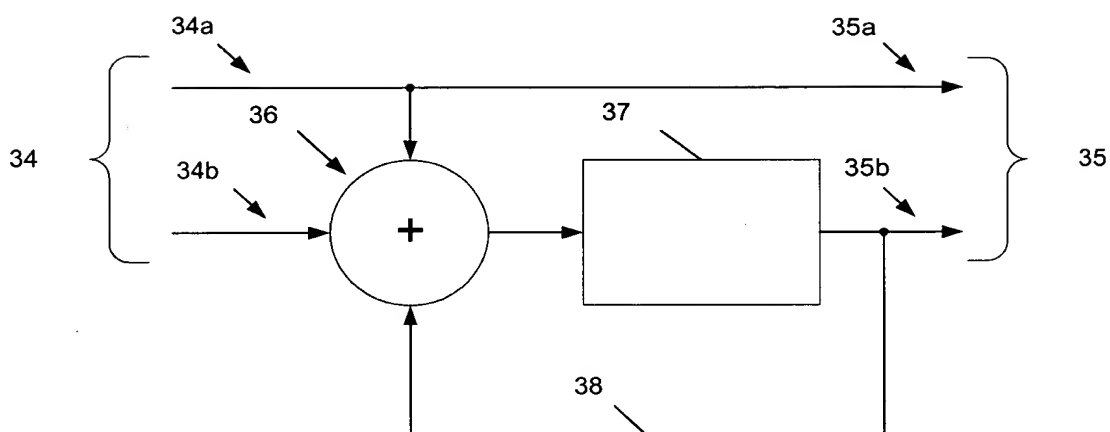


FIGURE 4

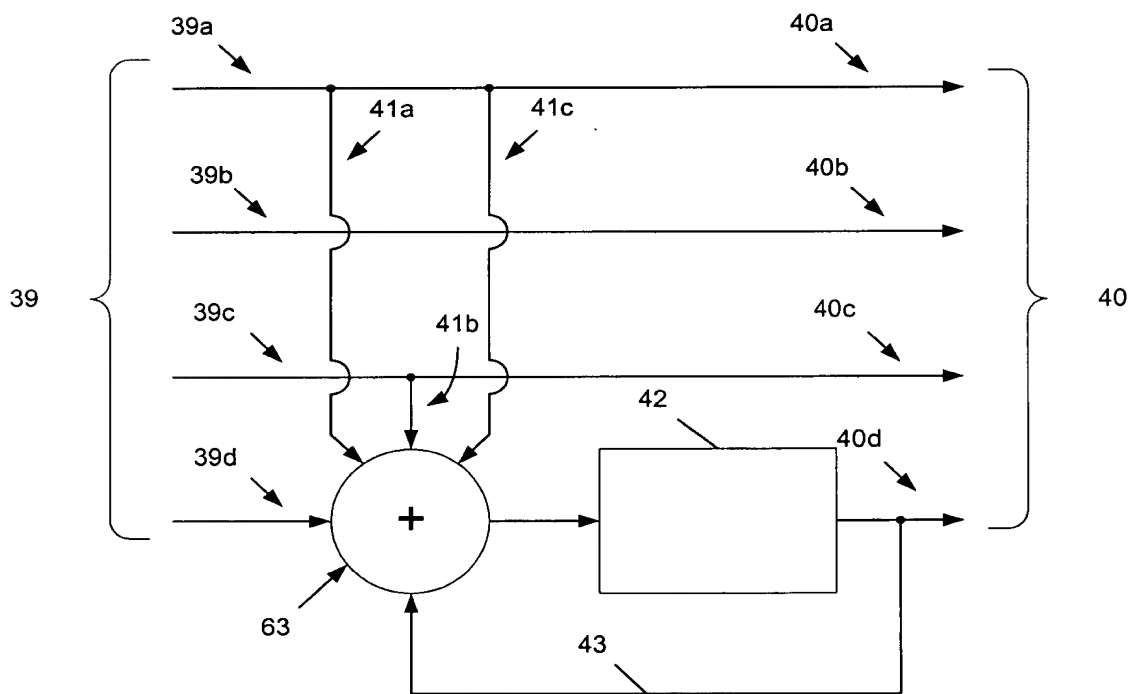


FIGURE 5

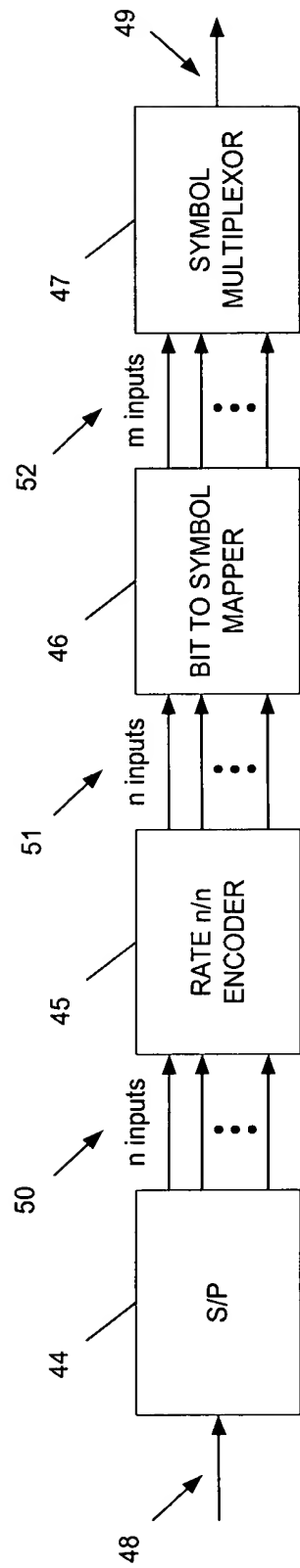


FIGURE 6

SECRET

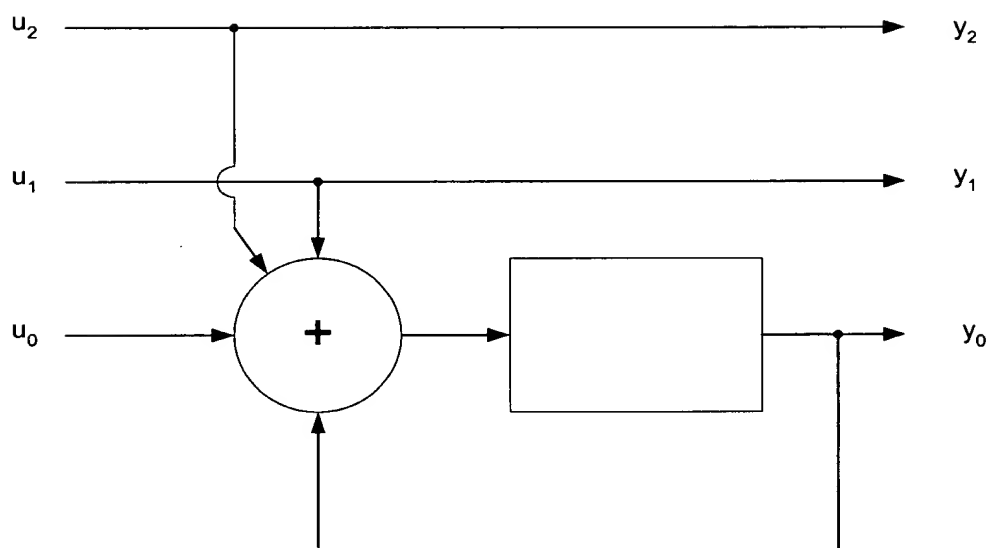


FIGURE 7A

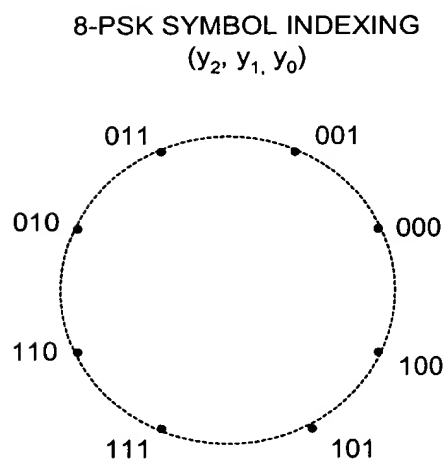


FIGURE 7B

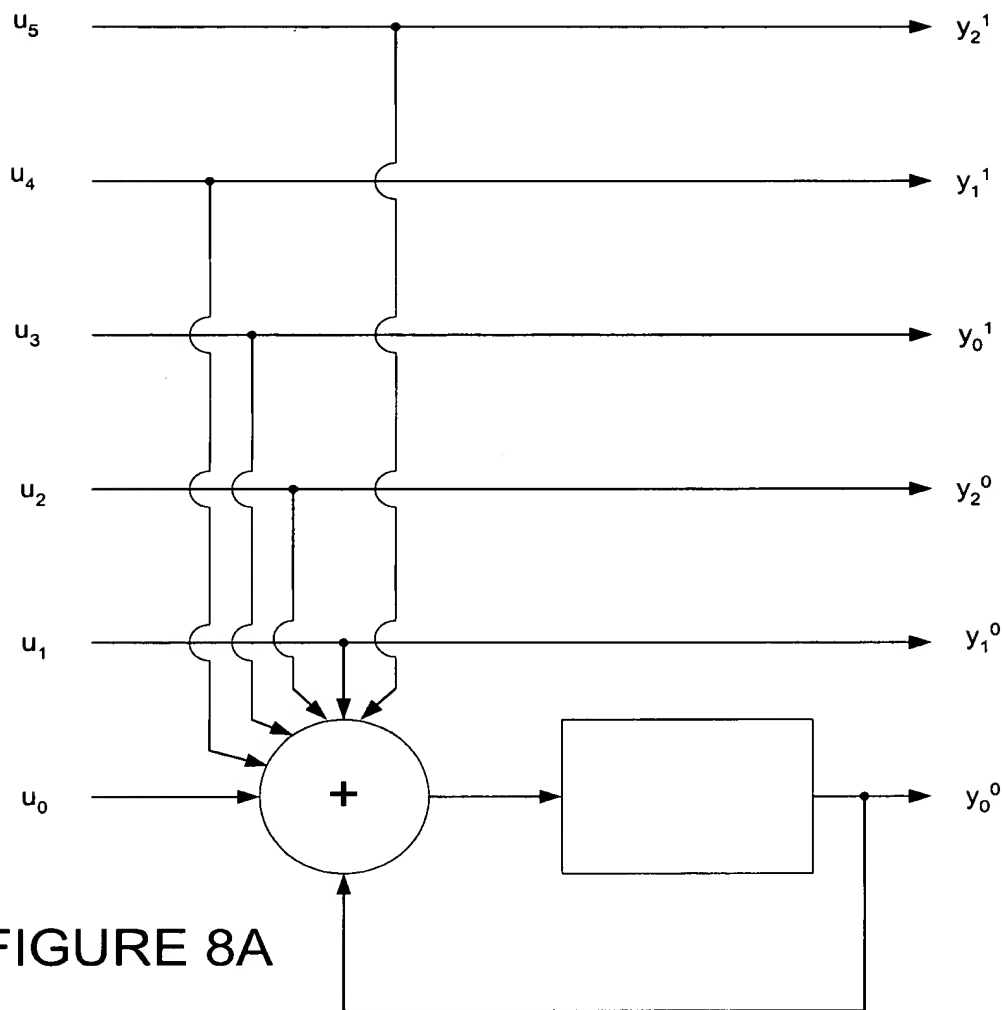


FIGURE 8A

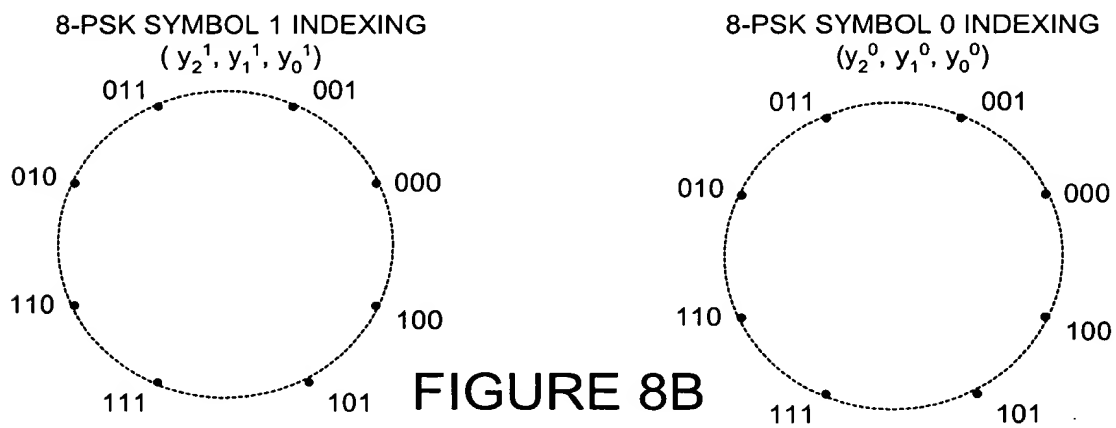


FIGURE 8B

SECRET

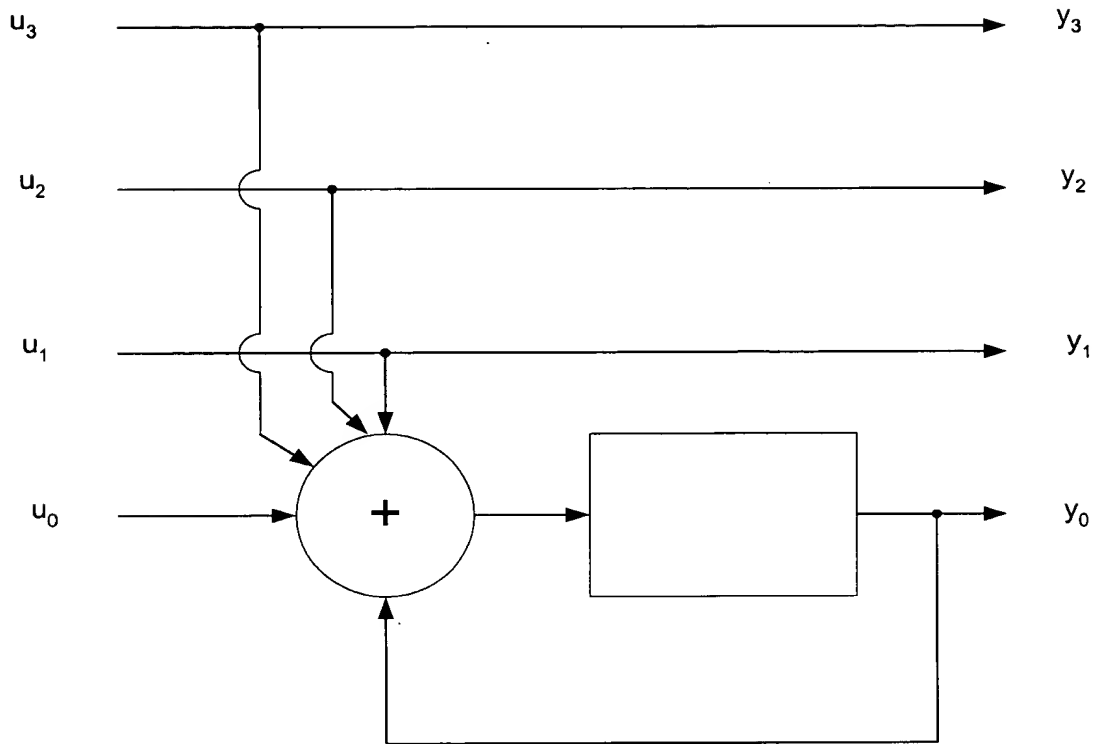


FIGURE 9A

16-QAM symbol indexing

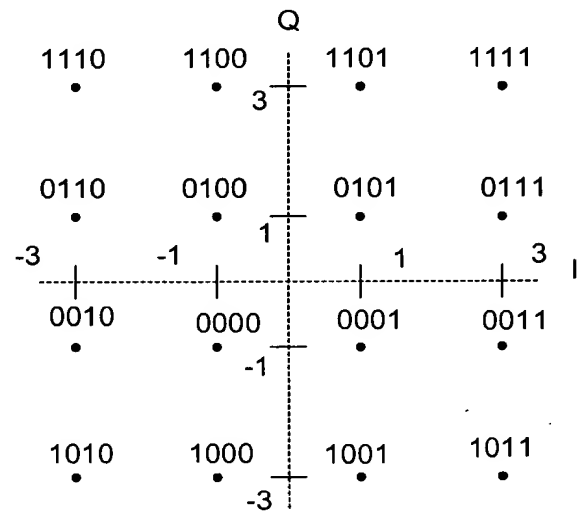
$$(y_3, y_2, y_1, y_0)$$


FIGURE 9B

00E290" 06920960

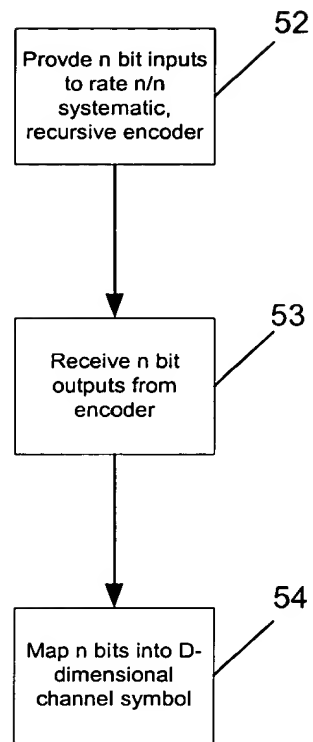


FIGURE 10

Rate 8/9 overall 8-PSK SCTCM performance: rate 3/3 inner code vs rate 6/6 inner code
15128-bit source data payload per block (BER floor estimated using Union Bound)

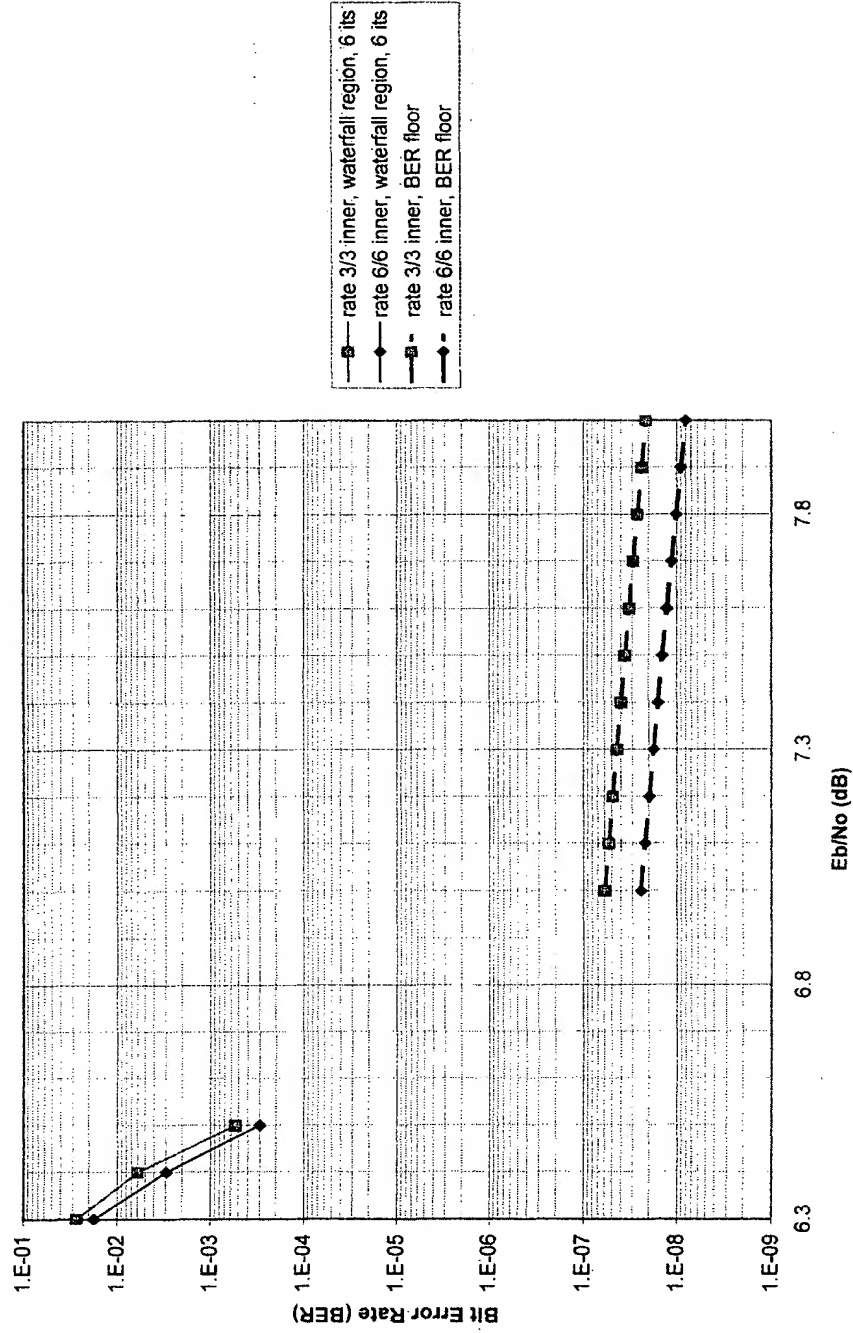


FIGURE 12C

Rate 2/3 Overall Waterfall Comparisons

Simulated (Waterfall) Performance
Rate 2/3 Overall, 15144 source bits, 5 iterations

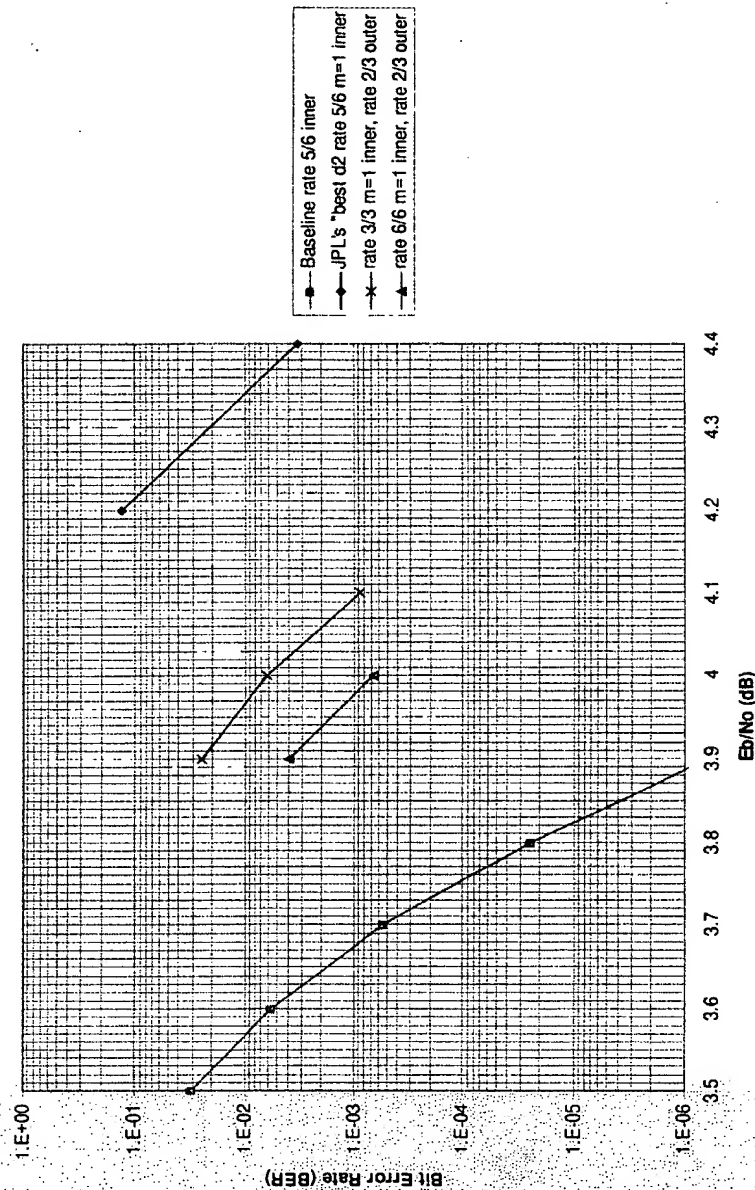


FIGURE 13A



Rate 5/6 Overall Waterfall Comparisons

Simulated (Waterfall) Performance
Rate 5/6 Overall (15147 source bits per block, 6 iterations)

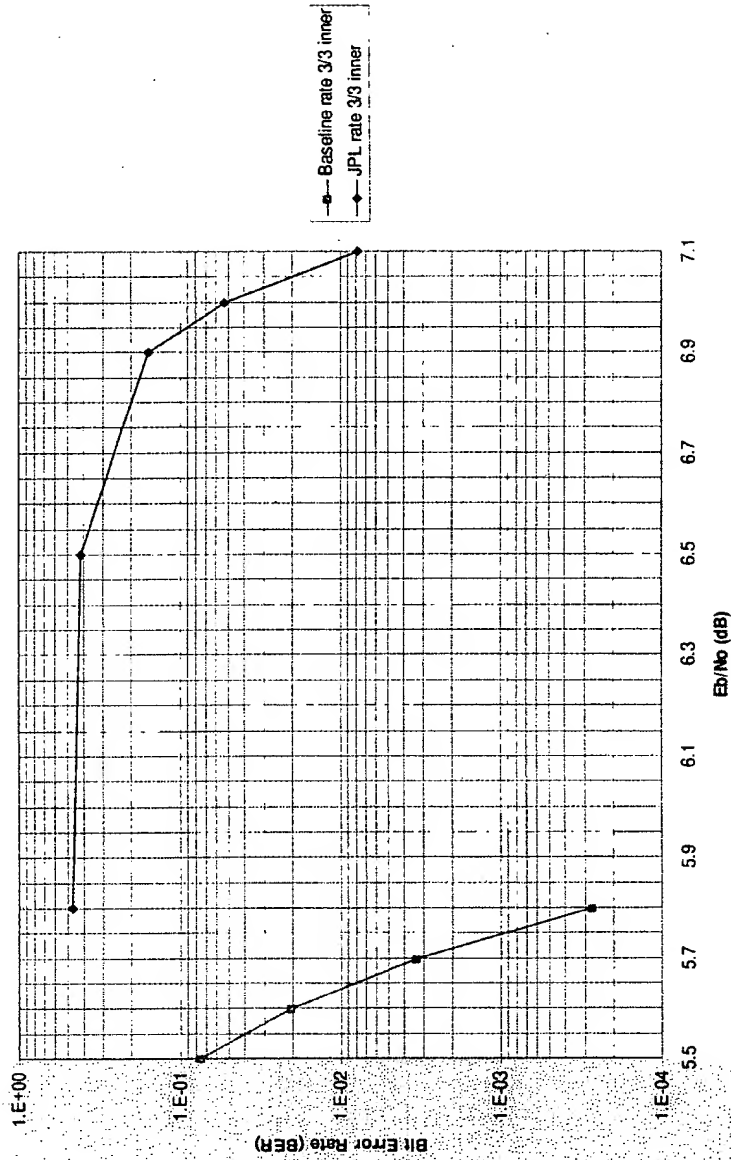
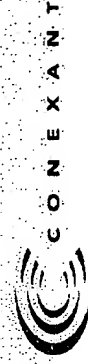


FIGURE 13B



Rate 3/3 vs Rate 6/6 Codes

Rate 5/6 overall 8-PSK SCTCM performance: rate 3/3 inner code vs rate 6/6 inner code

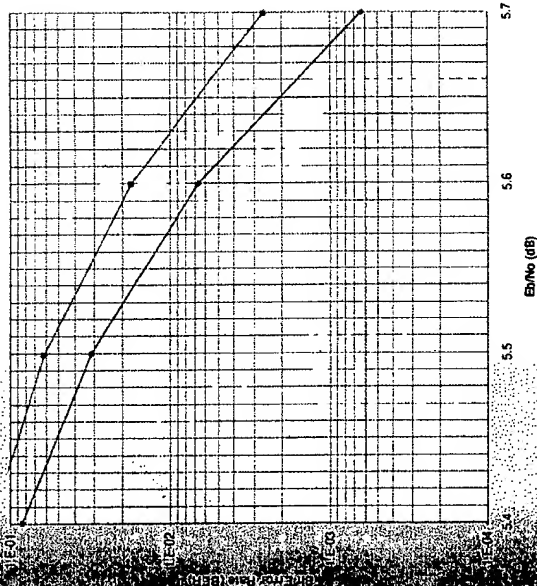


FIGURE 13C

Rate 8/9 overall 8-PSK SCTCM performance: rate 3/3 inner code vs rate 6/6 inner code

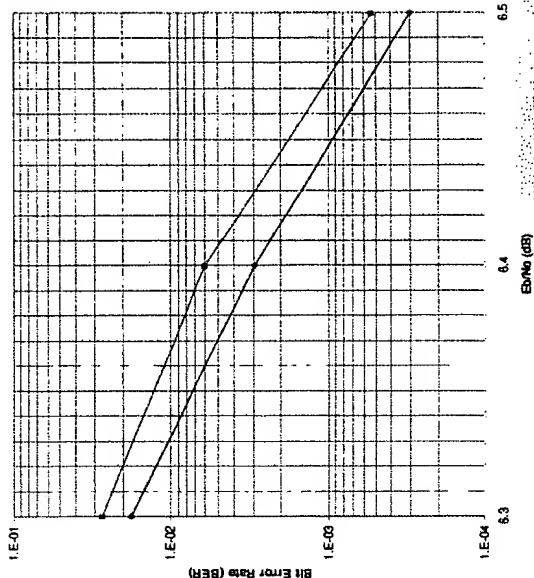


FIGURE 13D



CONEXANT

006290" 06920960

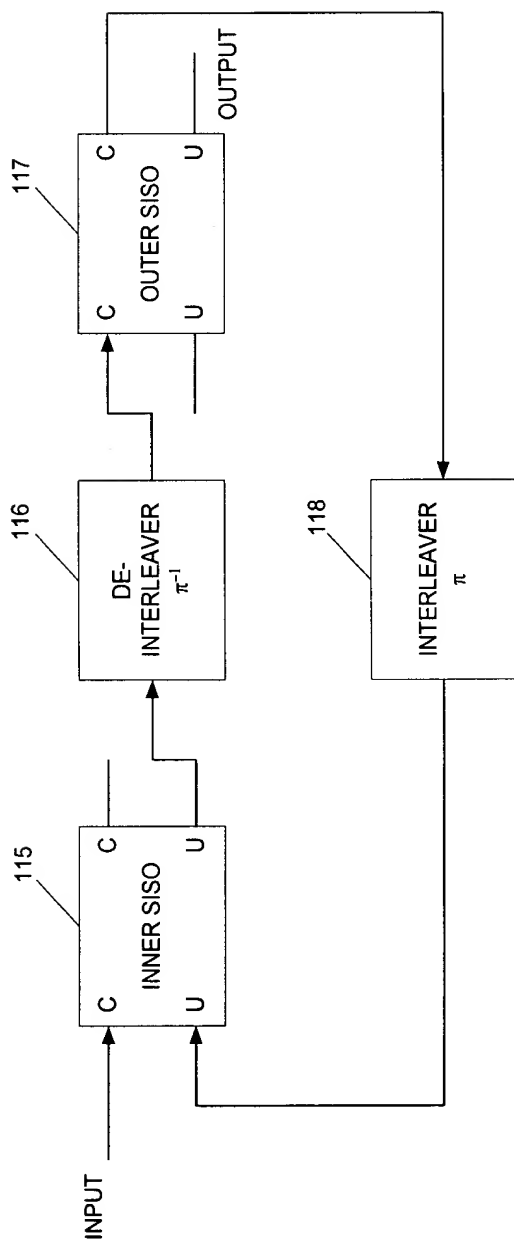


FIGURE 14

17



FIGURE 15

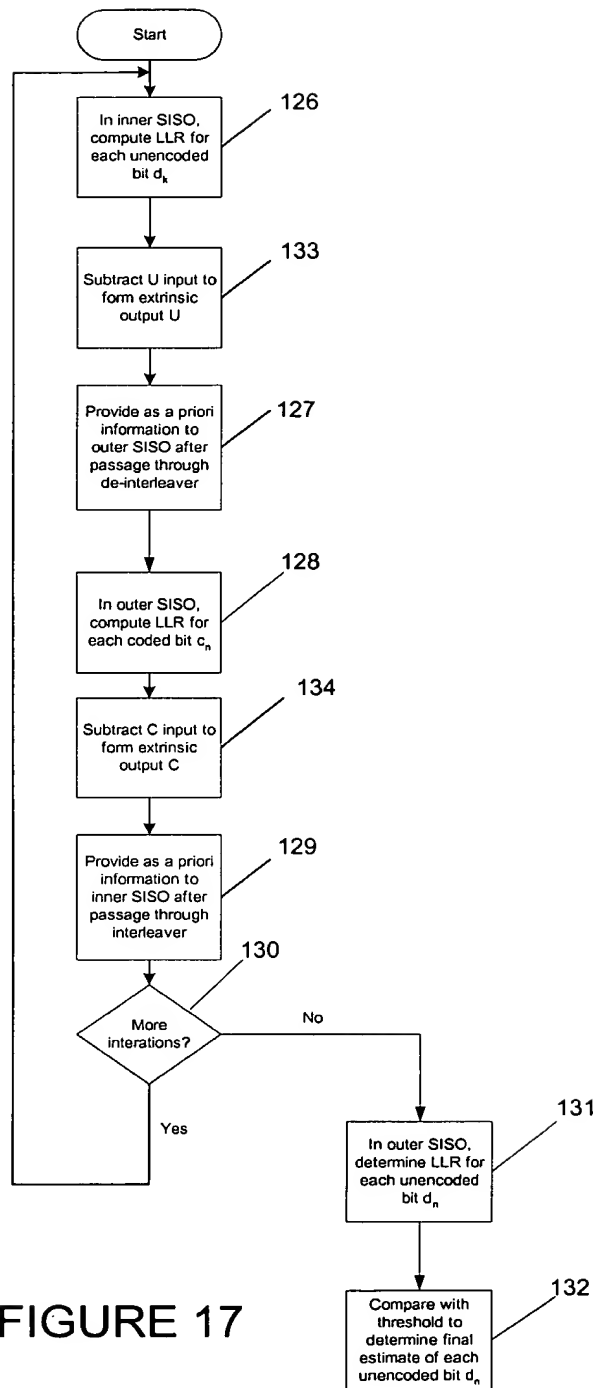


FIGURE 17